Hardware control systems - course description

General information

Course name	Hardware control systems
Course ID	06.2-WE-AutP-HCS-Er
Faculty	Faculty of Computer Science, Electrical Engineering and Automatics
Field of study	Automatic Control and Robotics
Education profile	academic
Level of studies	First-cycle Erasmus programme
Beginning semester	winter term 2019/2020

Course information

Semester	5
ECTS credits to win	3
Course type	optional
Teaching language	english
Author of syllabus	• dr inż. Michał Doligalski

Classes forms

The class form	Hours per semester (full-time)	Hours per week (full-time)	Hours per semester (part-time)	Hours per week (part-time)	Form of assignment
Lecture	15	1	-	-	Credit with grade
Laboratory	30	2	-	-	Credit with grade

Aim of the course

- to familiarize students with the basic techniques of specification, modeling and synthesis of hardware control systems
- to familiarize students with complex programmable structures
- shaping basic skills in the design of control systems using hardware description languages

Prerequisites

Foundations of digital and microprocessor engineerin , Discrete process control

Scope

Get acquainted with elementary digit systems. Basic logic gates. Basic digital flip-flops. Combined and sequential digital functional blocks (multiplexers, decoders / demultiplexers, counters, registers, memories). Decomposition of the digital circuit into the control and operating part. Methods of description of control and operating parts of the digital circuit. Cooperation of the operating system with the control system. Design of combination and sequential control systems using digital functional blocks. Design of digital control circuits using PLD, CPLD and FPGA programmable logic structures (introduction, internal design of PLD, CPLD and FPGA systems, design examples). Introduction to digital circuit design using hardware description languages (general VHDL model structure, VHDL VHDL example, VHDL language features, VHDL applications). Basic issues of VHDL language (model structure, data objects, data types).

Specification of digital behavior using process instructions (process structure, sensitivity list, basic sequential VHDL instructions, for example conditional statements and loops). Specification of the structure description of the digital system in VHDL (structural description elements, configuration instruction, replication statement, test procedure elements, test component instance, test vectors definition, assertion statement). Designing digital IPs (Intellectual Property) using VHDL. Application of VHDL language and programmable logic structures (PLD, CPLD and FPGA) in the design of digital control circuits

Teaching methods

Lecture: Conventional / Traditional Lecture

Laboratory: laboratory exercises using computer hardware

Learning outcomes and methods of theirs verification

Outcome description	Outcome symbols	Methods of verification	The class form
He can perform simulations and synthesis of simple binary control circuits		• a quiz • an ongoing monitoring during classes	• Laboratory
Has knowledge of programmable logic circuits		• an evaluation test	• Lecture
He is able to prepare a specification of basic functional blocks as a model in HDL		• a quiz • an evaluation test	• Lecture • Laboratory

Outcome description	Outcome symbols	Methods of verification	The class form
He is knowledgeable about methods of designing hardware control systems using hardware description languages (HDL)		• a quiz • an evaluation test • an ongoing monitoring during classes	• Lecture • Laboratory

Assignment conditions

Lecture - a condition of credit is to obtain positive grades from written or oral tests conducted at least once in a semester

Laboratory - a condition of credit is to obtain positive grades from all laboratory exercises, intended to be implemented within the laboratory program

Components of the final grade = lecture: 50% + laboratory: 50%

Recommended reading

1. Kamionka-Mikuła H., Małysiak H., Pochopień B.: Synteza i analiza układów cyfrowych, Wydawnictwo Pracowni Komputerowej Jacka Skalmierskiego, Gliwice, 2006
2. Łuba T., Zbierzchowski B.: Komputerowe projektowanie układów cyfrowych, WKiŁ, Warszawa, 2000
3. Pasierbiński J., Zbysiński P.: Układy programowalne w praktyce, WKŁ, Warszawa, 2001
4. Skahill K.: Język VHDL. Projektowanie programowalnych układów logicznych, WNT, Warszawa, 2001
5. Zwoliński M.: Projektowanie układów cyfrowych z wykorzystaniem języka VHDL, Wydanie 2, WKŁ, Warszawa, 2007

Further reading

1. Kalisz J. (Ed.): Język VHDL w praktyce, WKŁ, Warszawa, 2002.
2. Kalisz J.: Podstawy elektroniki cyfrowej, WKŁ, Warszawa, 1998.
3. Lisiecka-Frąszczak J.: Synteza układów cyfrowych, Wydawnictwo Politechniki Poznańskiej, Poznań, 2000.

Notes

Modified by dr hab. inż. Wojciech Paszke, prof. UZ (last modification: 05-05-2020 14:31)