Digital system design - course description

General information

Course name	Digital system design
Course ID	06.0-WE-INFP-DSD-Er
Faculty	Faculty of Computer Science, Electrical Engineering and Automatics
Field of study	Computer Science
Education profile	academic
Level of studies	First-cycle Erasmus programme
Beginning semester	winter term 2021/2022

Course information

Semester	3
ECTS credits to win	5
Course type	obligatory
Teaching language	english
Author of syllabus	• dr inż. Michał Doligalski

Classes forms

The class form	Hours per semester (full-time)	Hours per week (full-time)	Hours per semester (part-time)	Hours per week (part-time)	Form of assignment
Lecture	30	2	-	-	Credit with grade
Laboratory	30	2	-	-	Credit with grade

Aim of the course

- To provide basic knowledge about principles of fundamental Boolean and their application to digital design.
- To provide basic knowledge about combinational and sequential digital/logic circuits, and modular design techniques.
- To provide basic knowledge about data path and control unit design, and memory.
- To give basic skills in analysis and synthesis of logic circuits.

Prerequisites

Mathematical foundations of engineering, Logic for computer science, Experiment methodology I, Computer architecture I

Scope

Digital Computers and Information. Binary signals. Number systems, operations, and conversions: decimal, binary, octal, hex. Codes: BCD, parity, Gray. Combinational Logic. Logic gates. Logic functions. Standard forms: minterms/maxterms, SoP, PoS. Karnaugh maps. Two-level/Multilevel circuit optimization and implementations. Combinational Functions and Circuits. Decoders/Encoders. Multiplexers, implementation. Iterative Circuits. Binary Adder/Subtractors.

Sequential Circuits. Latches. Flip-flops. Finite State Machines. Mealy vs. Moore machines. Sequential Circuit Design: state assignment, designing with D and JK flip-flops. Registers. Registers with Load Enable and with Parallel Load. Register Transfers. Shift Registers, Shift Registers with Parallel Load, Bidirectional/Universal Shift Registers. Counters. Ripple Counters. Synchronous Binary Counters: design with D and JK flip-flops. Binary Up-Down Counter. Binary Counter with Parallel Load. BCD and Arbitrary Sequence Counters. Modulo N counters.

Introduction to VHDL Language.

Teaching methods

- Lecture, laboratory exercises.

Learning outcomes and methods of theirs verification

Outcome description	Outcome symbols	Methods of verification	The class form
Is aware of the dynamic development of the discipline		• a pass - oral, descriptive, test and other	• Lecture
Knows basic design methods for simple digital systems (specification, analysis and synthesis)		• a pass - oral, descriptive, test and other • carrying out laboratory reports	• Lecture • Laboratory
Can design simple combinational and sequential circuits		• an ongoing monitoring during classes	• Laboratory
Can run the synthesis of combinational circuits using digital functional blocks		• carrying out laboratory reports	• Laboratory

Assignment conditions

- Lecture – the passing condition is to obtain a positive mark from the final test.
- Laboratory – the passing condition is to obtain positive marks from all laboratory exercises to be planned during the semester.

- Calculation of the final grade: lecture 50% + laboratory 50%

Recommended reading

1. R.H.Katz, G.Borriello: Contemporary Logic Design, 2nd Edition, Pearson Education, 2005
2. K.Skahill: VHDL for Programmable Logic, Addison-Wesley Publishing, 1996
3. J.F.Wakerly: Digital Design, Principles and Practices, 4th Edition, Prentice-Hall, 2005
4. M.M.Mano, M.D.Ciletti: Digital Design, 4th Edition, Prentice-Hall, 2007\
5. M.Zwolinski: Digital System Design with VHDL, 2nd Edition, Prentice-Hall, 2003

Further reading

Notes

Modified by dr inż. Michał Doligalski (last modification: 08-09-2021 21:11)