Modelling and simulation of digital systems - course description

General information

Course name	Modelling and simulation of digital systems
Course ID	06.0-WE-INFP-MaSoDS-Er
Faculty	Faculty of Computer Science, Electrical Engineering and Automatics
Field of study	Computer Science
Education profile	academic
Level of studies	Erasmus programme
Beginning semester	winter term 2017/2018

Course information

Semester	5
ECTS credits to win	5
Course type	obligatory
Teaching language	english
Author of syllabus	• dr inż. Michał Doligalski

Classes forms

The class form	Hours per semester (full-time)	Hours per week (full-time)	Hours per semester (part-time)	Hours per week (part-time)	Form of assignment
Lecture	30	2	-	-	Credit with grade
Laboratory	30	2	-	-	Credit with grade

Aim of the course

- familiarize students with the standard languages of the equipment description (HDL)
- to familiarize students with the use of HDL languages for modeling, simulation, and synthesis of the digital circuits
- forming among students an understanding of the necessity of computer-based computing verification (simulation) of designed digital circuits

Prerequisites

Digital circuits, Fundamentals of programming, Computer architecture

Scope

Introduction: Genesis and destination of hardware description languages (HDL). Introduction to modeling of digital systems. VHDL language. General organization of the design unit. Different levels of abstraction describing the architecture of the design unit. Basic instructions parallel (instructions for assigning signal values, blocks, parallel instructions calling procedures and functions). Defining processes with a sensitivity list. Instructions Sequential. Synchronization of processes. The architecture of the unit presented in the form description of behavior (behavioral). The architecture of the unit in the form of a structure description. Configurations. Concepts of constants, variables and signals. Procedures and functions. Ways of the delay modeling. Attributes, predefined attributes. Packages. Libraries. Discussion complex types (records, files). Text operations in VHDL language. Creating models testers (testbench). Verilog language. General arrangement of the layout module. Abstraction levels of the module description. Basic parallel statements (continuous and procedural assignments, task calls and functions). Always and initial constructions. Sequential instructions. Modules. Models of systems in the form of structure description. Constants, networks and registers. Ways of delay modeling. The use of multivalent logic (high impedance modeling, creation three-state bus). Modeling of CMOS circuits. Standard gates and buffers. UDP systems: combinational and sequential. Tasks and functions. Tasks and system functions. Defining your own tasks and functions. Text operations in the Verilog language. The use of HDL languages for the synthesis of digital circuits. Modeling of machines digital. Strategies for designing digital systems in VHDL language. Sharing resources system. Delays in simulation and synthesis. Simulation including real delay (backannotation). Modeling of hardware and software systems. The basics of the SystemVerilog language.

Teaching methods

- Lecture: conventional / traditional lecture
- Laboratory: laboratory exercises using computer equipment

Learning outcomes and methods of theirs verification

Outcome description	Outcome symbols	Methods of verification	The class form
He can analyze the system digital at various stages design, including time parameters		• a quiz • an evaluation test	• Lecture • Laboratory
He can model a simple layout digital using the selected one hardware description language, including based on standard libraries as well IP-Core modules		• a quiz • an ongoing monitoring during classes	• Laboratory
He can use the equipment description languages in the design process of systems digital		• an evaluation test	• Laboratory

Outcome description	Outcomesymbols	Methods of verification	The class form
Rozumie potrzebę przeprowadzenia komputerowej weryfikacji (symulacji) projektowanych układów cyfrowych		• an evaluation test • an ongoing monitoring during classes	• Lecture • Laboratory

Assignment conditions

- Lecture - the condition for passing is to obtain positive marks from written tests or oral at least once per semester
- Laboratory - the condition for passing is to get positive grades from everyone laboratory exercises planned for implementation as part of the laboratory program, and knowledge tests, minimum two
- Components of the final grade = lecture: 50% + laboratory: 50%

Recommended reading

1. Zwoliński M., Digital System Design with VHDL, Prentice-Hall, Inc, 2003
2. Bergeron J.: Writing Testbenches using SystemVerilog, Springer, New York, 2006\
3. Cohen B.: VHDL Coding Styles and Methodologies, Kluwer Academic Publishers, Second Printing, 1996
4. IEEE Std 1364-2001: IEEE Standard Verilog Hardware Description Language, IEEE, Inc., New York, USA

Further reading

Notes

Modified by dr inż. Michał Doligalski (last modification: 04-04-2018 01:06)